REMARKS

This application has been reviewed in light of the Final Office Action mailed April 22, 2005. Reconsideration of this application in view of the below remarks is respectfully requested. Claims 1-6 are pending in the application with Claims 1 and 6 being in independent form.

I. Objection to Claims 1 and 6

Claims 1 and 6 are objected to for being difficult to understand. Claims 1 and 6 have been amended in a manner believed to clarify the phrasing in question.

II. Rejection of Claims 1-6 Under 35 U.S.C. §103(a)

Claims 1-6 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent No. 5,535,331 issued to Swoboda et al. (hereinafter, "Swoboda et al.") in view of U.S. Patent No. 6,732,307 issued to David Alan Edwards (hereinafter "Edwards").

Swoboda et al. teaches an integrated circuit (IC) emulator/simulator for IC design. The simulator of Swoboda et al. executes a software program that simulates an entire target chip, i.e., the target chip is a virtual representation, for cost-effective software development and program verification in non-realtime. (See col. 6, lines 41-45) This is quite different from Applicant's claimed invention, wherein a physical target chip, i.e. a CPU, is monitored during execution of a target program so that the actual behavior of the target chip can be traced in realtime.

Swoboda et al. fails to disclose or suggest: outputting an uncompressed instruction address as trace data when an instruction code of the instruction address/instruction code data is a branch instruction; outputting the uncompressed instruction address as the trace data when the section trace start signal from the event management means is active; and generating a plurality of compressed instruction addresses by compressing the instruction address of the instruction address/instruction code data, combining the compressed instruction addresses, and outputting

the compressed instruction addresses as the trace data when the instruction address of the instruction address/instruction code data is not a branch instruction and the section trace start signal is not active, as recited in Applicant's Claim 1.

The above-cited feature of the claimed invention allows trace data to not only be compressed, thus saving storage space, but also allows reconstruction of an instruction address even when the address is not a branch address.

Edwards teaches an apparatus and method for storing trace information. Specifically, Edwards discloses a debug circuit, which provides a number of signals, operable as preconditions for triggering particular events in the processor. These events may then generate trace data. However, there is no suggestion of selectively compressing trace data as recited in Claim 1.

Therefore, Swoboda et al. and Edwards taken alone or in any proper combination does not anticipate Applicant's Claim 1. Independent Claim 6 recites similar language to Claim 1. Accordingly, for at least the reasons presented above, Claims 1 and 6 are believed patentably distinct over the cited prior art references.

With regards to Claims 2-5, these claims are dependent from Independent Claims 1 and 6 and therefore are limited by the language recited by those independent claims. Accordingly, Applicant respectfully requests withdrawal of the rejection to Claims 1-6 under 35 U.S.C. §103(a) over Swoboda et al. in view of Edwards and allowance thereof.

III. Information Disclosure Statements

Regarding the previously submitted IDS, respectfully, Applicant is not required to submit a complete translation of foreign documents. 37 C.F.R. §1.98(a) recites, in part: "any information disclosure statement... shall include... a copy of the translation if a written English-language

translation of a non-English-language document, or portion thereof, is within the possession, custody, or control of, or is readily available to any individual designated in § 1.56(c)."

Further, in the case of prior art references cited during foreign prosecution, a translation into English of a statement from the foreign patent office stating the findings of the office with respect to the cited prior art is adequate for establishing relevance of that prior art. Therefore, it is believed that the Information Disclosure Statements as filed are sufficient and meet the minimum requirements of 37 C.F.R. §1.98(a).Accordingly, Applicant respectfully requests the consideration of all documents listed in the previously submitted Information Disclosure Statements in their entirety.

CONCLUSIONS

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-6 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Applicant's undersigned attorney at the number indicated below.

Respectfully submitted,

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